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Copper electrodes multilayer ceramic capacitors

Part II *Chips fabrication, optimisation and characterisation*

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In a companion paper, a ceramic formulation based on $CaZrO_3$ was developed to decrease the sintering temperature of this oxide. We achieved in obtaining a low sintering temperature ceramic fireable below the copper melting point while maintaining attractive properties whatever the atmosphere used (oxidising or reductive). The present paper deals with the fabrication of the copper electrodes multilayer ceramic capacitors (MLCC) and their optimisation. Several points have been tested to enhance the characteristics of the components. They are based on the precursors origin and the manufacturing process optimisation. These studies result in NPO components with good properties (C $\sim$ 30 pF/5 active layers; $\tau_\varepsilon = -45$ ppm/K; ESR $\sim$ 20 mΩ at 30 MHz; $tg\delta < 10 \times 10^{-4}$; $\rho_i > 10^{12}\ \Omega \cdot$cm).

1. Introduction

In a companion paper [1] (referred as I in the following), we have studied several ways to decrease the sintering temperature of the $CaZrO_3$ ceramics using sintering aids. The main result stands in a low sintering temperature ceramic fireable below the copper melting point (1083°C) while maintaining attractive properties. The samples sintered at 1000°C have a QF product of nearly 15, $\varepsilon \sim 28$, a near zero τ_ε and $\rho_i \sim 10^{12}\ \Omega \cdot$cm; these properties are roughly kept when the samples are sintered in a reducing atmosphere. The ceramic formulation is based on $CaZrO_3$ with $LiNO_3$, $CaCO_3$, SiO_2 and TiO_2 as sintering aids and high properties keepers.

In this paper, we are interested in the co-firing process, the fabrication of the copper electrodes multilayer ceramic capacitors (MLCC) using industrial precursors (ceramic precursors powders, metallic inks for the inner and outer electrodes, binders), the optimisation process and the chips reliability evaluation. It is divided in several parts more or less organised in a genetic order: (i) the study of the co-fired bulk ceramic with copper; (ii) the chips manufacturing with high purity precursors, their properties and the adjustment of the metallic inks used to form the electrodes (iii) the analysis of the precursors influence on the sintering and the high frequency properties; (iv) the chips manufacturing using the precursors selected in the previous point. Some components will also be described in these different paragraphs in term of defaults.

2. Experimental procedures

All of the synthesised powders and discs were analysed by X-Ray diffraction either with a Guinier's camera (ENRAF NONIUS FR590) or with a SEIFERT diffractometer (Copper's Kα_1 radiation).

Dilatometric measurements were carried out using a SETARAM TMA92 dilatometer. For all the measurements, the temperature ramp was heated and cooled at 2°/min with a dwell at 1350°C for one hour. A slight charge of 1 g was applied to allow the measurements.

The polished samples were observed using a polarised optical microscope (Olympus BH2-HLSH) or, after gold-sputtering, using a scanning electron microscope (Philips XL30 FEG SEM).

Phase composition analysis was determined using an energy dispersive spectrometer coupled with the SEM (EDS—Oxford Link ISIS).

The epsilon is measured by the Hakki and Coleman method [2]: a cylindrical sample is placed between two metal disks. When the disks come into contact with the cylindrical ends, the expression of the conditions of field's continuity gives a transcendental equation in Bessel function, which relates resonant frequency, permittivity and resonator dimensions.

The QF is determined using the mid-point width Δf of the resonance line and its frequency: $Q_0 = f_0/\Delta f$ [3]. To perform the measurement, the resonator is shielded in a silver plated cavity to eliminate the

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radiation. The cavity dimensions are at least three times the size of the dielectric resonator in order to ignore the metallic loss [4].

The ESR is measured with two transmission quarter-wave air-coaxial lines: a BOONTON line for the measurements at 30 MHz; an other BOONTON line for the measurements from 200 MHz to 2.6 GHz.

The insulation resistance (IR), quantifying the ability of a charge capacitor to withstand leakage in DC current is measured with a M1500 UFA (SOFELEC).

The capacitance and the dissipating factor of the components are measured with LCR Meter 410 ESI.

Until now, the only life test carried out is the endurance at 125°C for 2000 h.

3. Results and discussion

3.1. The co-sinterability

A stoichiometric $CaZrO_3$ phase was prepared using grade reagents (CERAC) $CaCO_3$ (99.95% purity) and ZrO_2 (99.95% purity). These two powders were wet-ball-milled in ethanol during 2 h in a Teflon recipient with zircon balls. The mixture was dried under infrared lamps and manually de-agglomerated in an agate mortar. This mixture was calcined in a tubular furnace (PIROX) at 1000°C during a 2 h dwell using a 150°/h heating/cooling rate. Then the two most interesting compositions were tested: composition C1 with an addition of 10 mol% $LiNO_3$ (Prolabo; 99%), 3 mol% $CaCO_3$ (CERAC; 99.95 purity) and 3 mol% amorphous SiO_2 (INC Biomedicals); composition C2 with an addition of 10 mol% $LiNO_3$, 5 mol% $CaCO_3$, 2.5 mol% amorphous SiO_2 and 2.5 mol% TiO_2 (Prolabo; 99%). The mixtures (i.e., the $CaZrO_3$ phase and the sintering aids) were prepared as previously exposed and an organic binder was added to the powder. It was uniaxially pressed into green discs into 8.06 mm (diameter) discs under a load of 3880 kg. The co-fired samples were prepared using in each case two discs (around 1 mm thickness). One face of each was painted with a mix of copper powder and organic binder. The painted faces were placed facing each other and the two discs were pressed together under a load of 3880 kg. The samples were sintered using a $10\%H_2/90\%Ar$ atmosphere moisture saturated at room temperature to avoid the metal oxidation. The sintering temperature was 1000°C. A dwell time of 6 h was imposed and the heating rate was 2.5 K/min. In both cases (using either composition C1 or C2) the results are comparable. The microstructure of the co-fired sample with composition C2 and the EDS analysis results obtained along a line crossing the interface ceramic/metal is shown in Fig. 1. The photograph indicates clean interfaces and the EDS analysis suggests no diffusion between the different layers (i.e, no diffusion from metal to ceramic or *vice et versa*). The EDS measurement threshold is 1 μm and, given this limit, one can say that no detectable diffusion occurs at the interface. Note that the apparent composition gradient effect for the silicon ion observed at the interface is a topographic artefact due to the groove between the ceramic and the metal. This groove also confirms the poor affinity between the two materials.

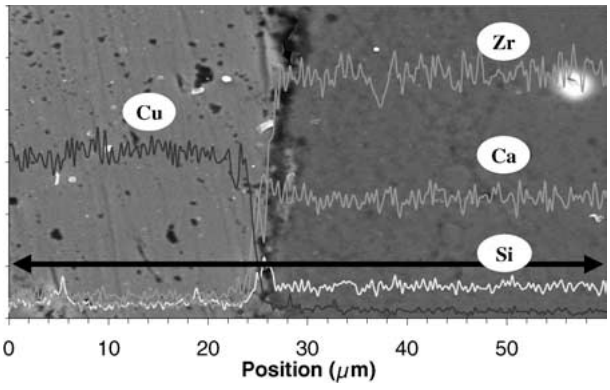

Figure 1 Microstructure of the co-fired sample with composition C2 and the EDS analysis results obtained along a line crossing the interface ceramic/metal. The dark bold line (with arrows) indicates the scanned path. The titanium analysis is not shown since it only exhibits a flat curve.

3.2. The prototype components

Considering both the low firing temperature and the co-sinterability of the ceramic with the copper, prototypes capacitors were manufactured. The ceramic composition retained for the tests was the composition C2 (i.e., the most unfavourable one considering the sintering temperature). The chips were manufactured by the TEMEX Society using the laboratory ceramic (based on high purity $CaCO_3$ and ZrO_2 precursors). The specific area of the ceramic powder was 5.41 m^2/g. A schematic view of the process [5, 6] is shown in Fig. 2. First, a slurry composed of the composition C2 and an organic binder (acrylic binder + polypale ester + softener) is prepared. For all the results debated in this paragraph, the binder percentage is 16%. The slurry is then made into tapes, cut (at 75°C) and painted with the copper ink. Here, two inks were tested with two different copper powders: a first one (Cu.i1) furnished by Kawasho (produced by CVD) and a second one (Cu.i2) from METALOR (produced by precipitation techniques) (for details, see Table I). In both cases, the organic binder was made of cellulose binder and kerosene. The tapes are then stacked, laminated and cut into chips. These firsts chips contain 6 metallic layers (five capacitive units). These components are sintered using the same

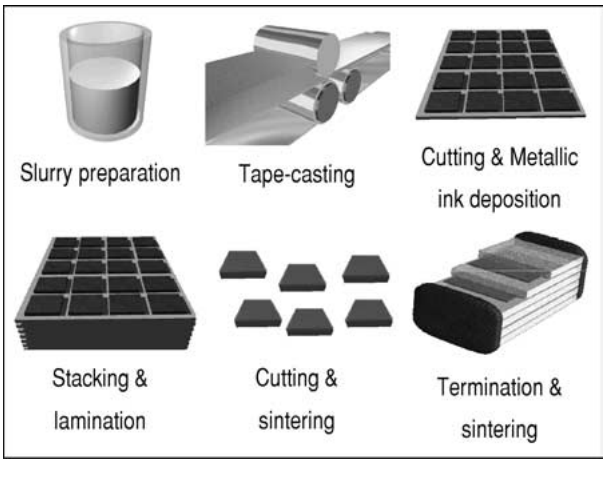

Figure 2 Schematic view of the chips fabrication.

TABLE I Metallic precursors characteristics (all the information are manufacturer data except the firing conditions. SA: Specific area in m^2/g; D50: average particle size in μm; BC: Burn out control; F: firing conditions used in this paper)

Name	Furnisher	Characteristics
Cu-I.i1	Kawasho	SA = 0.95; D50 = 0.71
Cu-I.i2 PNE CU58	Metallor	SA = 0.65; D50 = 4.7
Cu-I.e1 C4111K	Shoei Chemical INC	BC: easy; F = 910°C-3.33 K/min-6 min dwell; large particles
Cu-I.e2 C4118	Shoei Chemical INC	BC: a little difficult; F = 850°C-3.33 K/min-6 min dwell; small particles

reductive atmosphere as previously exposed. After sintering the outer-electrodes are deposited. Two kinds of inks were tested: C4111K (Cu.e1) and C4118 (Cu.e2) by Shoei Chemical Inc. (see Table I). Once again, the chips are fired to densify the terminations. The calcination step is important to avoid the blow of the chips. This step has been studied using the TGA analysis carried out on the organic binder used in the ceramic and the metallic ink, both in air and reductive atmosphere (the same as in paragraph 3.1). The results are shown in Fig. 3. They display that whatever the atmosphere used, almost all the binders are removed bellow 400°C. Concerning the metallic ink binder, it is surprising that the reductive atmosphere enhance the binder removal in the first part of the heating treatment (before 150°C), nevertheless, this result has been confirmed. Further TGA measurements were carried out on the chips with composition C2-Cu.I1. They slightly differ from the previous one with the departure at higher temperature of the NO_x from $LiNO_3$ and a slight weight loss at 800°C attributed to CO_2 removal from $CaCO_3$. These experiments also show a weight gain between 550 and 650°C when using the oxidising atmosphere. This can be attributed to the oxidation of the copper electrodes. Another oxidation step was observed at nearly 200°C by TGA analysis on the copper. According to this, the calcination was made at 400°C using the reductive atmosphere with a heating ramp of 0.3 K/min. and a cooling ramp of 2.5 K/min. The preliminary tests were carried out using chips with composition C2-Cu.i1-Cu.e1 and C2-Cu.i2-Cu.e1 to determine the optimal inner-electrode ink. The results obtained through dilatometric measurements using either an oxidising or reductive atmosphere are shown on Fig. 4a. The sintering cycle was +2.5 K/min to 1050°C, a dwell of 10 h and a cooling ramp as the heating one. These analyses were carried out in such a way to measure the shrinkage perpendicularly to the inner-electrodes. Being given the small thickness of the samples ($\ll$1 mm), the signal is badly noised. Nevertheless, this signal is sufficient to account for an almost similar behaviour as the one obtained with the bulk ceramic (Fig. 4b) with a shrinkage beginning at around 800–900°C and ending at temperature higher than 1050°C. The dwell seems to largely contribute to the shrinkage. The slow dilatation observed below 650°C is due to the binder removal. The large dilatation observed between 650 and 750°C could be due to the CO_2 removal from the calcium carbonate. This dilatation is more present using an oxidising atmosphere what could be due to a faster removal or maybe a departure of the carbon with different chemical composition (for instance CO_2 when using an oxidising atmosphere and CO when using a reductive one). No further experiments have been carried out to elucidate this point since it is out of the scope of this paper. The geometrical dimensions and the weight loss measured after

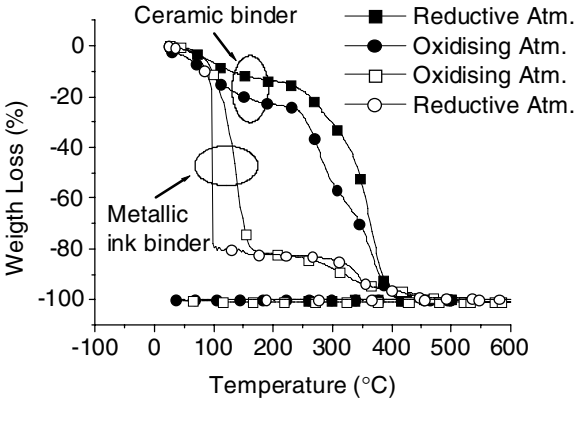

Figure 3 TGA measurements of the ceramic and metallic ink binders.

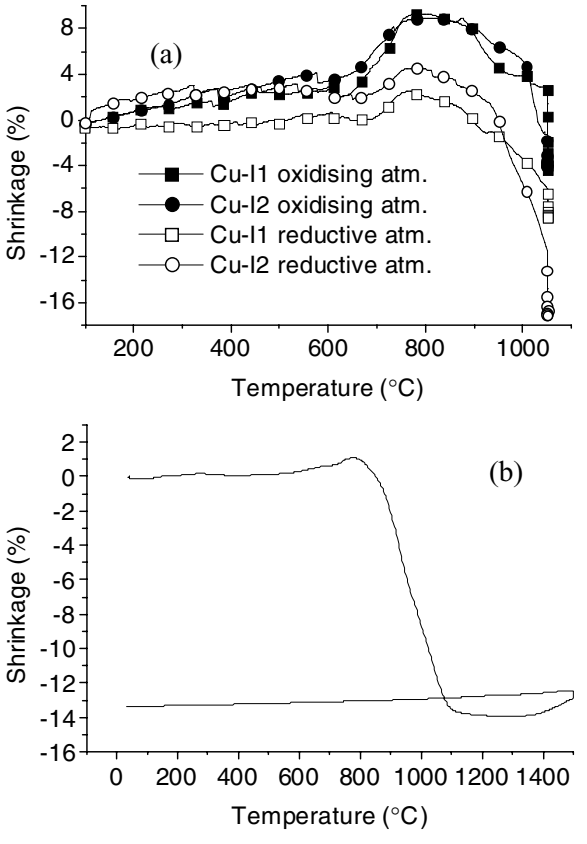

Figure 4 Dilatometric measurements of the chips as a function of the ink used for the internal electrodes in air and reductive atmosphere.

TABLE II Results of the dilatometric analysis as a function of the inner-electrodes ink and of the atmosphere

	Masse (%)	Thickness (%)	Width (%)	Length (%)	Densification (%)
C2-I.i1–Air	−14	−9.5	−14	−10	23
C2-I.i2–Air	−5	−20.5	−17	−12	64.5
C2-I.i1–H_2	−6.5	−17.5	−15.5	−13	43.5
C2-I.i2–H_2	−5	−25.5	−18.5	−20	97

the heating treatment are reported in Table II. Whatever the ink used for the inner-electrodes, the densification is more important when using the reductive atmosphere. The most interesting results are here obtained for the component with the Cu-I.i2 ink, which displays the highest densification rate with both atmospheres. It must be noted that the shrinkage seems to be more important in the thickness of this sample. Owing these results, the first sintering was made using a heating/cooling ramp of 2.5 K/min. A dwell of 6 h was maintained at 1060°C instead of 1050°C to enhance the densification. The sintering atmosphere was the same as the one used for the calcination stage. Note that the components were all encapsulated in an alumina crucible during the sintering stage. These tests account for a better behaviour obtained with the Cu-i1 ink: using the Cu-i2 ink, some delaminated components are present after the first sintering stage. This behaviour could be explained by the highly anisotropic shrinkage observed by the dilatometric measurements. Indeed, the inner-electrode could for instance shrink more rapidly with the I.i2 ink and when the ceramic begin to shrink, the metal could be sufficiently constrained (as a corrugated sheet) to push back the ceramic. Unwisely, such behaviour could not be observed, and either this explanation is false or the phenomenon is too discrete to be seen.

The second sintering stage with the ink Cu-e1 for the terminations was carried out using a 3.33 K/min rate for the heating/cooling ramp with a 6 min dwell at 910°C. The results obtained for the ESR (equivalent serial resistance) for both inks (using the better shaped components in the case of the Cu-i2 ink) are shown in Fig. 5. They confirm the above result with a lower ESR using the Cu-i1 ink (∼20 mΩ at 30 MHz). Since this property

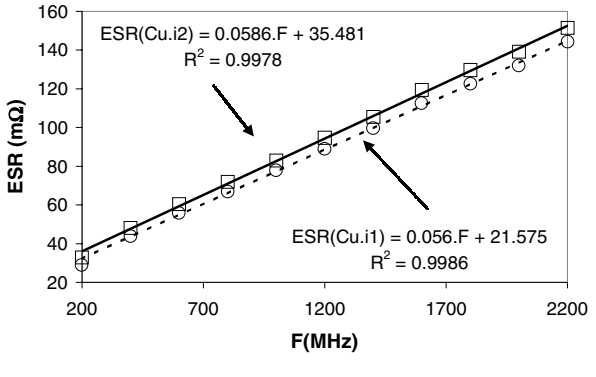

Figure 5 ESR measured as a function of the ink used for the internal electrodes (ESR in mΩ and F in MHz).

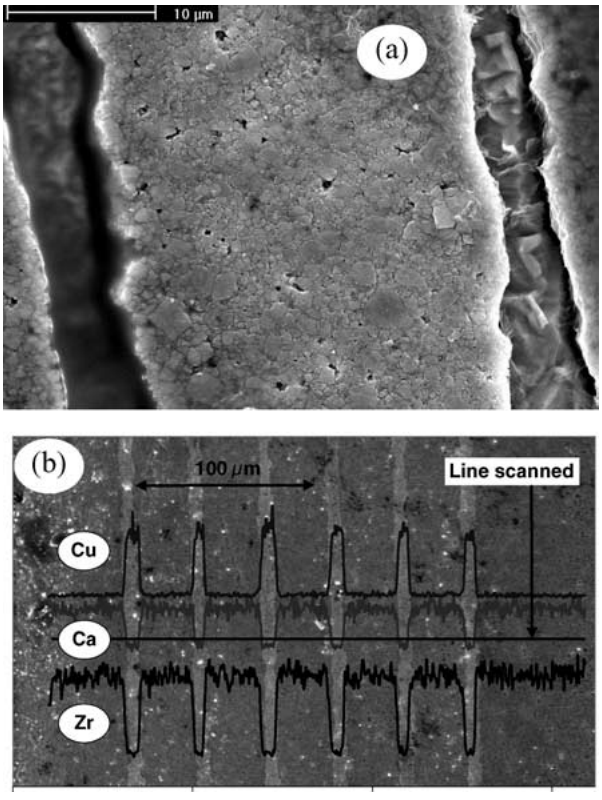

Figure 6 Microstructure of a chip with composition C2 and the EDS analysis results obtained along a line crossing the interfaces ceramic/metal. The dark bold line (with arrows) indicates the scanned path. The titanium analysis is not shown since it only exhibits a flat curve.

is largely influenced by the ceramic behaviour at low frequency, the quality of the contacts between the inner electrodes and the terminations and the conductivity in the metallic layers, three intermediate conclusions emerge: first, the ceramic behaviour at low frequency is very good which consolidates the choice for this dielectric composition; secondly, the contact between the inner and outer electrodes is satisfying; finally, since the ESR is slightly higher in the case of the use of the Cu-i2 ink, it is reasonable to say that some imperfections arise from this ink, which is in agreement with the previously observed results. The capacitance stability versus the temperature has been measured at 1 MHz. It is very high with a figure of 0 ± 45 ppm/K quoted across the temperature range −60°C–+180°C. In all the cases, the losses factor measured at 1 MHz was lower than 10×10^{-4} and the insulating resistance measured at 200 V was higher than $10^{12}\ \Omega \cdot$ cm. An example of such a component is shown in Fig. 6 with in (a), a chemically etched ceramic (using a mixture of 10% HF and 90% HNO_3) and in (b) the result of a line scan through an EDS analysis. The first figure account for a dense ceramic containing few remaining pores. The second one evidences no diffusion between the different layers (even at lower scale). Since the behaviour obtained with the ink Cu-i.1 was globally more suitable, the preliminary life-tests were carried out with such a composition (i.e., C2-Cu.i1-Cu.e1). The test consisted in applying a high voltage for several hours at 125°C (in air). 8 samples were tested using four different voltages (100, 200, 300 and 400 V). This test was carried out until the copper

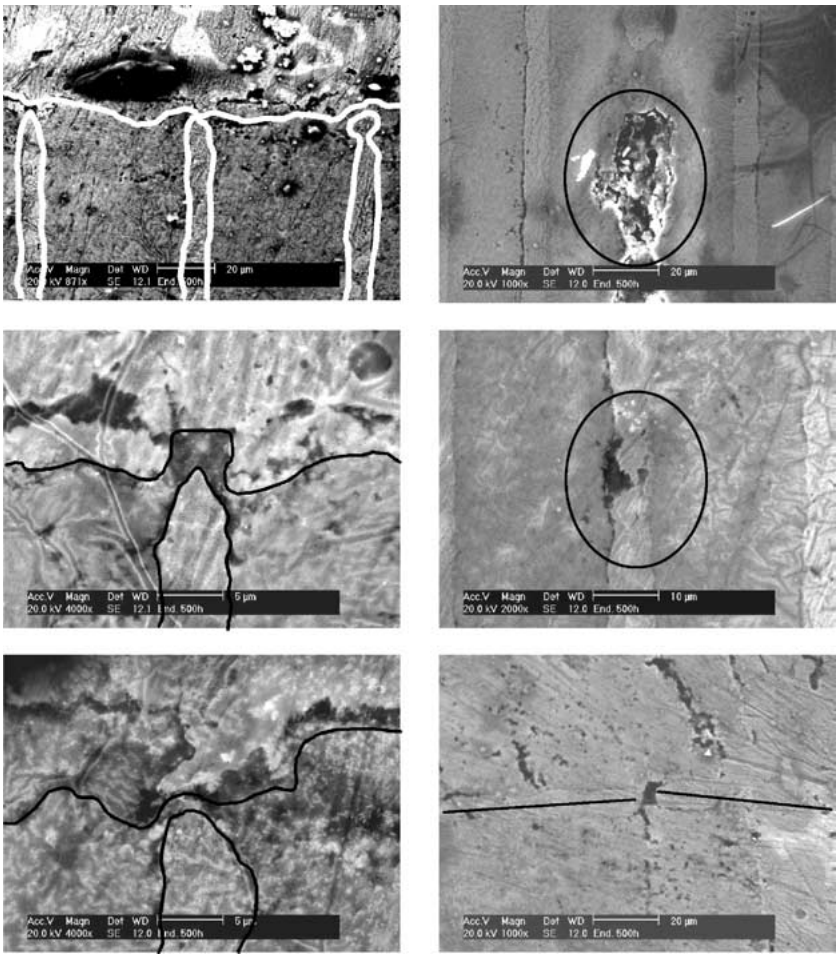

Figure 7 SEM micrographs of the chip presenting an endurance default after 500 h (C2-Cu.i1-Cu.e1).

electrodes begin to oxidise after 168 h. Whatever the applied voltage, no defaults appeared in the components. A second test was then carried out using electrolytic barriers (Ni + SnPb) to protect the copper terminations. Five chips were tested using the same temperature condition and applying a 200 V voltage. The first default appeared after 500 h with a chip displaying high losses and a decreased insulating resistance. This component presented several electrode imperfections as witness the microstructures shown in Fig. 7. From top to bottom and from left to right, it is shown that the contacts between the inner and outer electrodes are very thick. Moreover numerous large pores can be observed within the inner-electrodes. Finally, a torsion of one of the electrodes is also observable. It could result either from the mechanical constrains due to the fabrication process (cutting, lamination, . . .) or from those due to the by-hand manipulation of the components during the different steps of the elaboration and measurement. The second default appeared at the end of the test, after 2000 h of applied voltage at 125°C. It results in a lowering of the capacity ($\sim -6\%$) but neither an increase in the losses tangent nor or a decrease in the insulating resistance are observed. This kind of behaviour is generally attributed to contact problems between the inner and outer electrodes. Such defaults have been confirmed by SEM analysis, which have shown a low quality contacts between one of the inner-electrodes and a termination. The same kind of tests has been carried out changing the outer-electrodes ink (i.e., Cu.e2). All the components (5) have succeeded this test during 1100 h with an applied voltage of 200 V. Unwisely, the tests carried out at 300 V failed after 1212 h and the ones carried out at 400 V failed after 168 h. This seems to indicate that the nominal voltage for these components is around 100 V (the life-tests are done with a voltage equal to two times the nominal voltage). Finally, note that the only electrical difference observed between the two outer-electrode inks is in the temperature dependence of the capacitance. As already written, with the Cu-e1 ink, $\tau_\varepsilon = -45$ ppm/K while with the Cu-e2 ink, $\tau_\varepsilon = 0$ ppm/K. This good behaviour could be attributed to a higher densification of the outer-electrodes using this last ink (higher density predicted by the furnisher). Fig. 8 shows this difference in densification observed using the SEM.

3.3. The ceramic precursors influence

The dielectric composition was prepared using different precursors. All the tests were performed using the composition C1. The reagents characteristics are listed in Table III. For ZrO_2, five powders were tested, all presenting either different purities or average particles sizes or specific areas. The granulometric analysis results and the microstructure of these precursors are presented on Fig. 9. The results for D50 (average particle size) are in agreement with the data provided by the furnishers. Compared with the precursors used for the laboratory tests, the $CaCO_3$ particles size is around 2–3 times higher while the ZrO_2 one are markedly lower

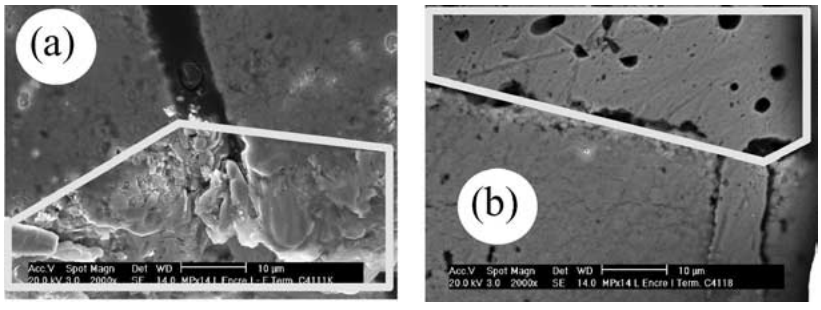

Figure 8 SEM micrographs of chips made of C2-Cu.i1 and (a) Cu.e1 or (b) Cu.e2.

(size as high as 80 μm for the CERAC's powder). The SiO_2 particles form large aggregates (D50 = 22.84 μm) but the observation of the microstructure reveals small particles (<100 nm). The great specific surface of the ZrO_2-C powder (Table III) is clearly explained by the microstructure that displays aggregates of very small particles (<50 nm). The less suitable ZrO_2 powder seems to be the A type with larges particles (>2 μm) aggregated in even larger heaps (>10 μm). The crystal structures determined through X-ray diffraction are all the same as the CERAC precursors for the crystalline phase ($CaCO_3$ and ZrO_2) and SiO_2 is confirmed to be amorphous. The composition C1 was then prepared with the different ZrO_2 powders and are named C1-A, . . . , C1-E with respect to the nomenclature given for the different ZrO_2 powders. In all cases, the X-ray patterns account for the formation of the $CaZrO_3$ phase. The powders have been milled two times (a first one to prepare the $CaZrO_3$ phase and a second one to prepare the C1 mixture), and the granulometric analysis evidence small particles with D50 around 600 nm for the compositions C1-A/B/E and 800 nm for C1-C/D. The microstructures observed using the SEM display small aggregates composed of smaller particles (diameter between 100 and 200 nm) except the C1-D powder that exhibits particles as large as 1 μm. All these samples have been analysed using the dilatometer and the results are shown in Fig. 10. It is noticeable that the two compositions that were initially presenting the most coarsened ZrO_2 particles (A/D) both display a dilatation at around 800°C. This behaviour has not been understood nevertheless it can be observed the dilatometric analysis for the two concerned samples result in a sintering temperature shifted to higher temperature. Table IV summarises the results observed using this analysis. The behaviour of the two above-mentioned samples could be detrimental for the chips fabrication. Indeed, the dilatation could shear the inner-electrodes and results in

TABLE III Ceramic pecursors characteristics

Precursor	Purity (%)	D50 (μm)	Specific surface (m^2/g)
$CaCO_3$	99.5 ± 1	20–35	0.3–1.5
SiO_2	99.8	35–50	
ZrO_2–A	99	12–16	4–6
ZrO_2–B	99.5	2.4	18–28
ZrO_2–C	99.9	1.12	33.2
ZrO_2–D	99.9	3.6	
ZrO_2–E	99.9	0.89	31

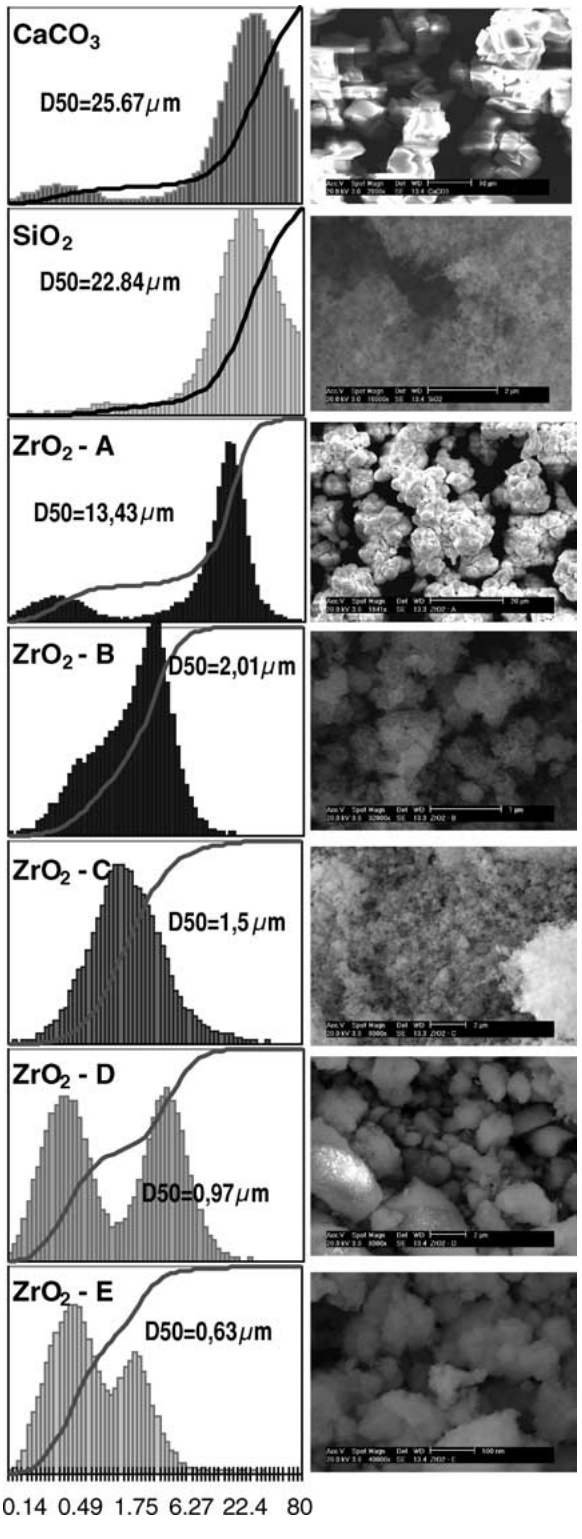

Figure 9 Characteristics of the precursors powders. Left: granulometric measurements; Rigth: SEM observation.

TABLE IV Compared results for the dilatometric analysis of the compositions C1-A/E. The reference for the comparison is the composition C1-CERAC. The table gives the difference in temperature observed at the shrinkage rate maximum and for the temperature resulting in a 90% shrinkage. The comments are the visual observations made on the dilatometric curves and on the samples after this heating treatment

Sample	T [Shrink. rate max.] (°C)	T [90% shrink.] (°C)	Comment
A	+40	+60	Dilatation-Fracture
B	+18	+13	
C	+5	−50	Weak shrinkage
D	+52	+6	Dilatation-Fracture
E	+34	0	

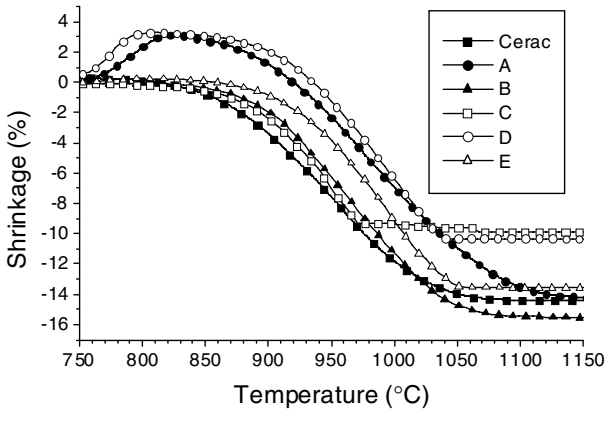

Figure 10 Dilatometric behaviour of the C1 compositions as a function of the precursors used.

either holed or very thick electrodes. The composition C1-C is not sufficiently densified, which prohibits its use in the MLCC. Note that its curious behaviour with an abrupt shrinkage break has been confirmed to be reproducible. The most interesting compositions are C1-B and C1-E. The first one exhibits a slight increase in the sintering temperatures (compared to the laboratory composition based on high purity CERAC precursors), both at the shrinkage rate maximum (+18°C) and at the end of the shrinkage (+13°C), while the second one only exhibits a delay at the shrinkage rate maximum (+34°C). All these samples were sintered in the Ar/H_2 mixture moisture saturated at room temperature at 1000 and 1050°C (heating/cooling ramp of 2.5 K/min; dwell of 6 h). The dielectric properties measured in the microwave domain are shown in Fig. 11. As observed using the dilatometer, the samples with composition A and D are fractured whatever the sintering temperature (1000 or 1050°C). These samples could not thus be accurately measured: no permittivity measurement could be achieved and the Q factors (having an important uncertainity) are only presented for comparative purposes. Nevertheless, these measurements are given to show the tendency of the measured properties. Undoubtedly, the best results are obtained with the high purity CERAC precursors. These samples display both the highest permittivity and a high Q factor; they also display a good stability versus the sintering temperature. The Q factor for the composition C1-A is low (∼1000) but offers a satisfying stability. The properties for the composition C1-B are interesting but slightly

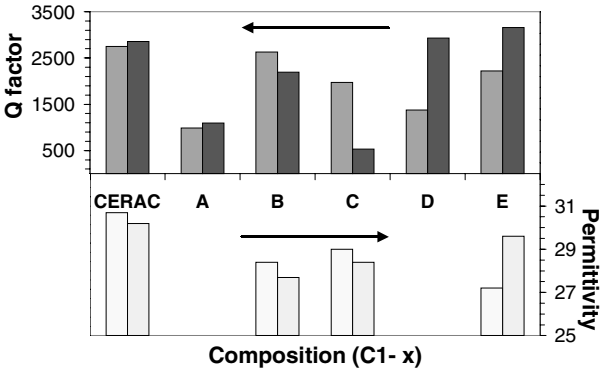

Figure 11 Dielectric properties of the C1 compositions sintered in reductive atmosphere either at 1000°C (left bars) or at 1050°C (right bars) as a function of the precursors used.

lower than the ones of the laboratory prototypes. Note that among all the tested compounds (except the prototypes), this composition is the one that offers the best stability versus the sintering temperature. The C1-C composition displays an attractive permittivity whatever the sintering temperature but its Q factor is largely influenced by the heating treatment; in any case, this Q factor is one of the lowest. As already mentioned, no permittivity measurement could be achieved for the C1-D composition. Its Q factor is very dependent upon the sintering temperature and is almost doubled when increasing this temperature of 50°C. The composition C1-E is also sensitive to the sintering temperature with a gain of about 2.5 in the permittivity and nearly 50% in the Q factor (2200 → 3200) with the increasing of the sintering temperature. Owing to this analysis, the ZrO_2-B precursor has been retained to manufacture the chips.

3.4. Chips manufacturing using the industrial precursors

The same process as previously exposed was retained to make the components with composition C1-Cu.i1-Cu.e2. The main difference stands in the adjustment of the amount of organic binder used for the ceramic tapes preparation. This step was necessary to obtain mechanically reliable components. Indeed, using the previous conditions (16 wt%), the tapes tended to stick to the lamination tools. The binder amount has been increased little by little to obtain a tape with sufficiently good mechanical characteristics and an as low as possible amount of binder. This choice for a low binder concentration is justified by the necessity to find a compromise between the mechanical needs and the binder removal without inflating the component in the first thermal stage (calcination). The optimal amount was found to be 20% of binder. Paraffin oil (1.5%) was used to facilitate the separation of the ceramic tape from its plastic support. Note that during the lamination stage, a rubber was used to avoid the sticking between the ceramic tapes and the tool. No delamination was observed on the green chips. Tests carried out using other binders were unsuccessful. The observations of this green chips revealed that the electrodes were

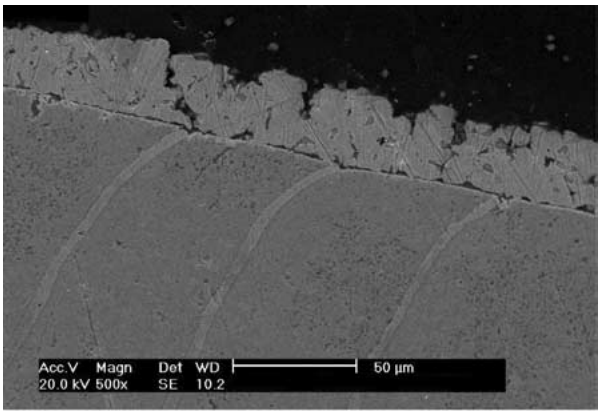

Figure 12 Curved inner-electrodes and contact default between the inner and outer-electrodes.

slightly curved near the extremities of the components. In order to correct this curvature, which was shown to be deleterious to the contact between the inner and outer electrodes (as illustrated in Fig. 12), the cutting temperature was decreased to 45°C. It resulted in well-shaped components. Since the amount of binder was increased and in order to optimise its removal, the calcination step was realised both in air (up to 300°C) and the upper mentioned reductive atmosphere (as already said up to 400°C but now using a heating ramp of 9 K/min). These tests have shown that an oxidising atmosphere was detrimental to the components with some delaminations. The first sintering (without the outer-electrodes) was again carried out at 1060°C. The second one depends of the metallic ink used (Table I). The microstructures observations account for the good shrinkage of the ceramic (>25%) and the inner electrodes (∼50%). Unwisely, they also account for a poor contact between the inner and outer electrodes. Since the only difference between the prototype made of laboratory ceramic and the one made of the industrial precursors stands (within the process and excluding a contribution from the precursors) in the binder amount, further tests have been carried out to understand why it was necessary to increase this amount and in which way it was disturbing the manufacturing process. It thus has been shown that the lithium nitrate was responsible for the bad behaviour during tape casting and the lamination process. Indeed, this material is severely hygrophilous, which results in an increased adherence to the tools. In this way, increasing the binder amount had permitted to limit this behaviour but in the other hand, the slight over-inflation in the ceramic induced by the addition of 4% of binder during the calcination stage was detrimental to the two following thermal stage, with the withdrawal of the inner-electrodes inside the component that was unwisely maintained after the first sintering stage prohibiting the contact between the inner and outer-electrode in the last stage. Several solutions have been envisaged to thwart this problem: (i) pre-calcinate the powders in order to eliminate the nitrates (ii) replace $LiNO_3$ by an other material presenting an almost similar behaviour (Li_2CO_3 for instance [7]), (iii) highly dry this precursor (iv) or even process the tape casting, cutting and lamination in an almost dry atmosphere, . . . The main results stands in the fact that we know that the dielectric formulation is compatible with the application concerned, that some prototypes were designed and have good properties, that the technology can be industrially used and that efforts must be now made in order to improve the manufacturing process.

4. Conclusion

The dielectric composition developed in I was successfully made into multilayer capacitors. It is shown that the quality of the component highly depends of the precursors used for both the ceramic and the inner/outer electrodes. The best components fabricated exhibit very good properties with a high capacitance (∼30 pF with 5 capacitive layers of nearly 20 μm in thickness), a low linear temperature coefficient (−45 ppm/K), a low ESR (∼20 mΩ at 30 MHz), low dielectric losses ($<10\times10^{-4}$) and a high insulating resistance ($>10^{12}$ Ω). The firsts endurance tests are very promising since the only observed defaults originate from the manufacturing process. Further experiments have been planed to improve the process in order to obtain homogeneous batches of components.

References

1. M. POLLET and S. MARINEL, *J. Mater. Sci.*, submitted.
2. B. W. HAKKI and P. D. COLEMAN, *IRE Trans. Microwave Techn.* (1959) 402.
3. Y. KOBAYASHI and M. KATOH, *IEEE Trans. Microwave Theory Techn.* **MTT-33**(7) (1985) 586.
4. J. M. DURAND and P. Y. GUILLON, *Electron. Lett.* **22**(2) (1986) 63.
5. International Patent no. WO 98/25281.
6. R. E. MISTLER and E. R. TWINAME, "Tape Casting: Theory and Practice," edited by the American Ceramic Society (Newman, 2000) [ISBN 1-57-498029-7].
7. M. POLLET, S. MARINEL and G. DESGARDIN, *J. Europ. Ceram. Soc.*, in press.

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